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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

July 1 to September 30, 1972

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, July 1 to September 30, 1972

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
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NBS Technical Notes are designed to supplement the Bureau's regular publications program. They provide a means for making available scientific data that are of transient or limited interest. Technical Notes may be listed or referred to in the open literature.

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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,* the Defense Nuclear Agency,† the U.S. Navy Strategic Systems Project Office,§ the U.S. Navy Electronic Systems Command,+ the Air Force Weapons Laboratory,¶ the Air Force Cambridge Research Laboratories,# the Atomic Energy Commission,** and the National Aeronautics and Space Administration.†† Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the program is reflected in planning and conduct of the work.

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* Through Research and Technical Services Cost Centers 4251126, 4252128, and 4254115

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+ Through Project Order PO-2-1034. (NBS Cost Center 4252534).

¶ Through Delivery Order F29601-71-F-0002. (NBS Cost Center 4252535).

Through Project Order Y72-873. (NBS Cost Center 4251536).

** Division of Biology and Medicine. (NBS Cost Center 4254425).

†† Through Order S-70003-G, Goddard Space Flight Center and Order H-87437-A, Marshall Space Flight Center. (NBS Cost Centers 4254429 and 4254447).

METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
JULY 1 TO SEPTEMBER 30, 1972

This quarterly progress report, seventeenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include design of a plan to provide standard silicon wafers for four-probe resistivity measurements for the industry, publication of a summary report on the photoconductive decay method for measuring carrier lifetime, publication of a comprehensive review of the field of wire bond fabrication and testing, and successful completion of organizational activity leading to the establishment of a new group on quality and hardness assurance in ASTM Committee F-1 on Electronics. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; and measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes. New efforts were initiated in both the die attachment and wire bond evaluation tasks. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes. A description of breakdown tracks, a primary failure mode of monolithic integrated circuits stressed with voltage pulses, is given in a separate appendix.

Key Words: Aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); recombination centers; resistivity; ribbon wire bonding; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; trapping centers; ultrasonic bonding; wire bonds.

1. INTRODUCTION

This is the seventeenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. The Program is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Normally, the technical services provided to other government agencies are simply listed in Appendix C. However, in providing technical services to one of these agencies a phenomenon was encountered which was deemed sufficiently important to warrant separate discussion in Appendix E. One of the most prevalent modes of failure of monolithic integrated circuits exposed to voltage transients is a breakdown track which shunts one or more p-n junctions. There is relatively little information available concerning this failure mode; some of it is contradictory. Without a better awareness and understanding of this failure mode, little progress is apt to be made in making monolithic devices more resistant to voltage transients and overvoltages such as may occur due to, for example, line-voltage surges and transients, improper testing procedures, and a variety of effects of intense electromagnetic environments.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include (1) design of a plan to provide for the industry standard silicon wafers for four-probe resistivity measurements, (2) publication of a summary report on the photoconductive decay method for measuring carrier lifetime, (3) publication of a comprehensive review of the field of wire bond fabrication and testing, and (4) successful completion of organizational activity leading to the establishment of a new group on quality and hardness assurance in ASTM Committee F-1 on Electronics. In addition new efforts were initiated in both the die attachment and wire bond evaluation tasks.

Highlights of these and other on-going activities are presented in this section; details of progress in technical areas are given in subsequent sections of the report. This section concludes with a summary of standardization activities being carried out by program staff members.

Resistivity — Work is continuing on the development of procedures for substantiating both provisional and regular certification of silicon wafers to be provided to the industry as standard reference materials for use in conjunction with the four-probe method for measuring resistivity. Informal industry consensus was achieved for accepting an initial provisional certification of ±10 percent. The temperature coefficient of resistivity has been tabulated for both *n*- and *p*-type silicon near room temperature. Several changes are being introduced in the experimental and analytical procedures used to obtain capacitance-voltage data and to calculate doping profiles in order to improve the quality of the measurement.

Generation-Recombination-Trapping Centers — Various expressions for the storage time in diode reverse-recovery measurements of carrier lifetime have been compared; applicability of certain expressions indicates when geometrical corrections must be used. The reproducibility of lifetime as determined by the surface photovoltage (SPV) method was studied, and long-term drift in values was observed. Further studies of the effect of heat treatment on the resistivity of silicon slices continued.

Gold-Doped Silicon — The activation energy of the gold donor in silicon has been obtained from the results of measurements of the Hall coefficient over the temperature range 140 to 320 K on silicon wafers doped with boron and gold. Activation energies in the range 0.3609 to 0.3627 eV were found on specimens with gold densities of 3.9×10^{15} to 1.1×10^{17} cm^{-3}; the origins and significance of the small differences in energy observed have not yet been established.

Infrared Methods — The infrared response (IRR) spectra of eight lithium-drifted germanium gamma-ray detectors were measured and identification was made of which of the five IRR spectrum groups they correspond. Further analysis of this body of

spectra has been deferred while a search of the pertinent literature is being carried out to aid such an analysis. Efforts to extend the use of the IRR technique to commercial small-volume semiconductor devices continued; IRR measurements were made on three silicon devices.

Die Attachment Evaluation — The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in semiconductor devices using the TRUMP computer thermal analysis program was postponed because of a delay in getting a copy of a revised version of the program. The fabrication of new test circuits to measure transient thermal response of power transistors in both the diode and transistor operating modes was completed. Initial measurements of thermal response of transistors operated in the diode-connected mode revealed that devices with excessively poor die attachment tended to heat up causing a decrease in power dissipation during the applied heating pulse. Nevertheless the thermal response was a satisfactory measure in locating devices with voids. Three groups of transistor chips were bonded to headers with intentionally introduced controlled void areas for experiments to obtain quantitative data on the relationship between thermal response and voids in transistor die attachment.

Wire Bond Evaluation — Measurements of pull strength of unannealed and annealed aluminum wire bonds as a function of pull rate continued, but the analysis is not yet complete. Experimental study of factors affecting the pull test on two-level bonds was begun. Work on the fabrication of aluminum balls for bonding was resumed. A report summarizing the work on ribbon wire is being prepared. The preparation of an annotated bibliography of limited distribution reports on bonding continued.

Thermal Properties of Devices — Measurements made on a variety of different types of power transistors to compare the emitter-only switching technique with the emitter-and-collector switching technique confirmed that the emitter-only switching technique is preferred for measuring thermal resistance of power transistors. The investigation of several unusual observations made on devices susceptible to severe current constrictions continued with consideration of their effect on the screen for hot spots based on measurements of common-emitter current gain.

Microwave Device Measurements — The study of conversion loss measurement repeatability was continued, but measurements were interrupted by erratic operation of the modulation attenuator, which required extensive repairs. Standard deviations were calculated for all recent measurement runs, and the application of statistical control charts to these measurements was started. An important equation relating conversion loss measurement uncertainty to modulator attenuation uncertainty was derived. A comprehensive report on work to date has been started.

Carrier Transport in Junction Devices — A large part of project activity was again devoted to assembling equipment and establishing techniques for measuring transistor high-frequency scattering parameters (S-parameters) at the wafer level. A technique for checking the phase-angle calibration of a vector voltmeter was developed, and a method for verifying the overall operation of a delay-time system employing the vector voltmeter was tested using R-C delay-time networks on TO-5 headers. Good agreement was obtained between the measured and calculated electrical behavior of R-C delay-time networks on TO-72 headers intended to be circulated as part of a forthcoming interlaboratory comparison of S-parameter measurements.

Standardization Activities — Standardization activities directly related to particular task areas are reported with the appropriate tasks. However, many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities, which are reported here, involve general staff support in committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway.

Nine program staff members attended the regular fall meeting of ASTM Committee F-1 on Electronics at Scottsdale. Following the Scottsdale meeting, a new test procedure on etch pit determination in germanium was drafted and one test method was edited.

Considerable effort was expended in the organization of a new group within Committee F-1 to address measurement problems associated with assurance of radiation hardness of semiconductor devices. This group, established in response to a request by the Defense Nuclear Agency, has as its chairman Dr. James Williams of Sandia Laboratories and as its secretary Dr. William Willis of Aerospace Corporation. More than 60 representatives of both the semiconductor device and the radiation effects communities attended the organizational meeting and selected four areas — test patterns for metallization evaluation, d-c and low frequency device characteristics, high-frequency and fast pulse device characteristics, and photocurrent — for immediate attention. The organizational effort was coordinated with the Radiation Effects Committee of the IEEE Group on Nuclear Sciences and liaison with appropriate groups in EIA-JEDEC, SAE, and other government agencies was maintained.

Four program staff members participated in the Navy Workshop on Device Reliability at Warrenton, Virginia, in July. Test methods and standards at all levels of fabrication and procurement were widely recognized as essential contributors to future improvements in reliability.

Most activity in connection with EIA-JEDEC Committees concerned thermal measurements. In addition to the activity reported elsewhere (see sec. 5.1.), program

staff members attended meetings of Committees JC-22 on Rectifier Diodes and Thyristors and JC-25 on Power Transistors.

The *ad hoc* Committee on Materials and Processes for Electron Devices of the National Materials Advisory Board (NMAB) recently issued two reports. One covers the research problems that appear to exist with various electron device materials in which the Department of Defense has an interest, and the other deals with problems in production of semiconductor devices. In the first report, *Materials and Processes for Electron Devices* (NMAB-289),* the committee concluded that where silicon is a candidate material for developmental work in electron devices, it is likely to be preferable to alternatives even though the extreme requirements being placed on it in some applications have exposed a number of areas that will have to be strengthened before it reaches its full potential. The committee also concluded that "the impact of an organized program to make in-process measurements [for the manufacture of silicon semiconductor devices] could be truly immense. All aspects of the electronics industry would be upgraded by higher yields, quality, and reliability. The increased understanding of device processing would allow pursuit of goals that are presently unattainable because of geometrical or reliability limitations (microwave, displays, memories, etc.)."

In the second report, *Yield of Electronic Materials and Devices* (NMAB-290),* it was recommended, among other things, that special attention be paid to improved specification and procurement practices and that a government-industry committee to coordinate work for high-reliability semiconductor-production procedures be created. High priority was placed on the initiation of research for both improved processes and improved, preferably non-destructive, tests for quality in the key areas of metallization, die and wire bonding, plastic encapsulation, and hermetic packaging. In the area of reliability assurance, highest priority was assigned to programs designed to "establish more meaningful and economical screens that are materials/process oriented rather than component oriented" and to "study new techniques for more effective production control of materials and processes."

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* Copies of this report can be obtained from the Printing and Publishing Office of the National Academy of Sciences, 2101 Constitution Avenue, N.W., Washington, D. C. 20418.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Work is continuing on the development of procedures for substantiating both provisional and regular certification of silicon wafers to be provided to the industry as standard reference materials for use in conjunction with the four-probe method for measuring resistivity [1]. Informal industry consensus was achieved for accepting an initial provisional certification of ±10 percent. The temperature coefficient of resistivity has been tabulated for both *n*- and *p*-type silicon near room temperature. Several changes are being introduced in the experimental and analytical procedures used to obtain capacitance-voltage data and to calculate doping profiles in order to improve the quality of the measurement.

Silicon Resistivity Standards — Plans were developed to offer standard reference materials to the industry for resistivity measurements. Sets consisting of two silicon wafers, one with resistivity about 0.1 Ω•cm and the other with resistivity about 10 Ω•cm would be provided. The resistivity of both wafers would bear provisional certification of ±10 percent. These plans were discussed at the September meeting of the Resistivity Section of ASTM Committee F-1 on Electronics and were judged adequate to begin the program. A general preference was expressed that the certification be based on measurement of each wafer rather than on a batch sampling procedure.

Although provisional certification at the 10 percent level can be based on existing data including the results of past round-robin experiments [2], new multilaboratory experiments must be carried out to establish the levels to which standard samples ultimately can be certified. Several organizations experienced in performing resistivity measurements have agreed to furnish data on their standard samples to NBS over the first 18 months of the program so that the necessary data base can be obtained. Others may also participate in this collaborative program and thereby couple their capabilities and measurements more directly into the industry-wide system. Details of the procedures to establish provisional certification are being developed, the multilaboratory comparison program is being designed, and specifications for the silicon crystals required for this program are being prepared.

(J. R. Ehrstein)

Other Standards Activities — The eighth of nine participating laboratories is now measuring the specimens in the round-robin experiment being conducted in

Table 1 — Temperature Coefficient of Resistivity of Silicon in the Range 18 to 28°C

Resistivity (Ω·cm)	Temperature Coefficient (Ω·cm/Ω·cm·°C)		Resistivity (Ω·cm)	Temperature Coefficient (Ω·cm/Ω·cm·°C)	
	n-type	*p*-type		*n*-type	*p*-type
0.0006	*0.00200*	*0.00160*	1.0	0.00736	0.00707
0.0008	*0.00200*	*0.00160*	1.2	0.00747	0.00722
0.0010	*0.00200*	0.00158	1.4	0.00755	0.00734
0.0012	0.00184	0.00151	1.6	0.00761	0.00744
0.0014	0.00169	0.00149	2.0	0.00768	0.00759
0.0016	0.00161	0.00148	2.5	0.00774	0.00773
0.0020	0.00158	0.00148	3.0	0.00778	0.00783
0.0025	0.00159	0.00145	3.5	0.00782	0.00791
0.0030	0.00156	0.00137	4.0	0.00785	0.00797
0.0035	0.00146	0.00127	5.0	0.00791	0.00805
0.0040	0.00131	0.00116	6.0	0.00797	0.00811
0.0050	0.00096	0.00094	8.0	0.00806	0.00819
0.0060	0.00060	0.00074	10.	0.00813	0.00825
0.0080	0.00006	0.00046	12.	0.00818	0.00829
0.010	-0.00022	0.00031	14.	0.00822	0.00832
0.012	-0.00031	0.00025	16.	0.00824	0.00835
0.014	-0.00026	0.00025	20.	0.00826	0.00840
0.016	-0.00013	0.00029	25.	0.00827	0.00845
0.020	0.00025	0.00045	30.	*0.00828*	0.00849
0.025	0.00083	0.00073	35.	*0.00829*	0.00853
0.030	0.00139	0.00102	40.	*0.00830*	0.00857
0.035	0.00190	0.00131	50.	*0.00830*	0.00862
0.040	0.00235	0.00158	60.	*0.00830*	0.00867
0.050	0.00309	0.00208	80.	*0.00830*	0.00872
0.060	0.00364	0.00251	100.	*0.00830*	0.00876
0.080	0.00439	0.00320	120.	*0.00830*	0.00878
0.10	0.00486	0.00372	140.	*0.00830*	0.00879
0.12	0.00517	0.00412	160.	*0.00830*	0.00880
0.14	0.00540	0.00444	200.	*0.00830*	0.00882
0.16	0.00558	0.00471	250.	*0.00830*	0.00884
0.20	0.00585	0.00512	300.	*0.00830*	0.00886
0.25	0.00609	0.00548	350.	*0.00830*	0.00888
0.30	0.00627	0.00575	400.	*0.00830*	0.00891
0.35	0.00643	0.00596	500.	*0.00830*	0.00897
0.40	0.00656	0.00613	600.	*0.00830*	*0.00900*
0.50	0.00678	0.00639	800.	*0.00830*	*0.00900*
0.60	0.00696	0.00659	1000.	*0.00830*	*0.00900*
0.80	0.00720	0.00687			

conjunction with ASTM Committee F-1 to determine interlaboratory precision of four-probe resistivity measurements on silicon epitaxial layers deposited on substrates of opposite type. Although data are being reduced and tabulated as received, a revised summary will not be made until the experiment is completed. (F. H. Brewer)

Values of C_T, the temperature coefficient of resistivity near room temperature, have been tabulated for both *n*- and *p*-type silicon. The values, listed in table 1, are based on the polynomials (NBS Tech. Note 560, pp. 6-7):

$$C_T = \sum_{n=0}^{k} A_n (\ln \rho)^n \qquad (1)$$

where ρ is the resistivity in ohm-centimetres, A_n are the appropriate coefficients and k is 17 for *n*-type and 13 for *p*-type silicon. These polynomials were developed with the requirement that at no point within the resistivity range 0.001 to 500 Ω·cm would the value of C_T derived from the polynomial deviate by more than 0.0002 deg^{-1} from the curve drawn through the experimental data [3]. The tables have been extended down to 0.0006 Ω·cm and up to 1000 Ω·cm by taking smoothed values to avoid oscillations of the polynomials in these extreme regions. Smoothed values are indicated in italic type in the table. The intervals were chosen so that intermediate values within the maximum deviation specified above could be obtained by linear interpolation. (J. R. Ehrstein)

Capacitance-Voltage Methods — The study of ways to reduce the observed discrepancies between resistivity of bulk slices as measured by the four-probe and capacitance-voltage (C-V) methods continued. Preliminary results (see 3.2.) of the study of the effect of the heat cycle during diffusion on the resistivity of the wafer suggest that noticeable resistivity change can occur particularly in specimens with carrier density $\lesssim 10^{15}$ cm^{-3}. This result led to the decision to make the four-probe resistivity measurement on the back side of the wafer after removal of the oxide and diffused layers on this side by lapping and before metallization. Introduction of the lapping and metallization steps into the processing is also expected to improve the quality of the C-V measurements by eliminating the back-side capacitor and lowering the contact resistance.

Other ways to improve the quality of the C-V measurements were also considered. A new algorithm [4] to correct the measurements for peripheral and diffused-layer effects is based on experimentally determined values of sheet resistance and junction depth. Fabrication procedures have been altered so that future wafers will be accompanied by pilot slices on which those characteristics can be measured directly. Computer programs are being developed to use this algorithm to compute doping profiles from C-V data, assuming one of several diffusion profiles. The program based on a gaussian diffusion profile has been completed.

In addition, the probe stand is being modified to exclude room light during measurements, to improve electromagnetic shielding, and to increase the electrical stability of the probe and diode. These changes are expected to increase the accuracy with which capacitances can be measured. (R. L. Mattis and M. G. Buehler)

Plans: A general procedure for testing probe force in four-probe arrays, based on previously reported information (NBS Tech. Note 743, pp. 8-9), will be prepared for ASTM Committee F-1. If the measurements are completed, the results of the round robin on the four-probe measurement of epitaxial layer resistance will be summarized for presentation at the January meeting of ASTM Committee F-1. Collection and screening of silicon crystals with regard to resistivity uniformity and oxygen content for suitability as resistivity standard slices will begin. Procedures for control and management of the program will be developed and the starting date announced. On completion of the organization of the resistivity standards program, study of the current and probe force dependence of four-probe measurement of resistivity of epitaxial silicon will be resumed. The effects of the various changes in experimental and analytical procedures begun this quarter will be evaluated in the effort to achieve better agreement between four-probe and C-V resistivity measurements.

3.2. GENERATION-RECOMBINATION-TRAPPING CENTERS

Objective: To develop electrical measurement methods, mathematical models, and test structures for characterizing the electronic properties and density of generation-recombination-trapping (GRT) centers in silicon, with emphasis on methods applicable to control of characteristics such as lifetime and leakage current.

Progress: Various expressions for the storage time in diode reverse recovery measurements of carrier lifetime have been compared; applicability of certain expressions indicates when geometrical corrections must be used. The reproducibility of lifetime as determined by the surface photovoltage (SPV) method was studied, and long-term drift in values was noted. Study of the effect of heat treatment on the resistivity of silicon slices continued.

Diode Recovery Methods — Expressions for the reverse recovery transient associated with short base diodes have been evaluated. The base width (W) of a diode is defined as the distance between the p-n junction and the contact to the more lightly doped region where the lifetime is assumed to be zero. The relationship between the ratio of the storage time (t_s) to the minority carrier lifetime (τ) as a function of the forward to reverse current ratio (I_f/I_r) which follows from the exact series solution of the diffusion equation [1]:

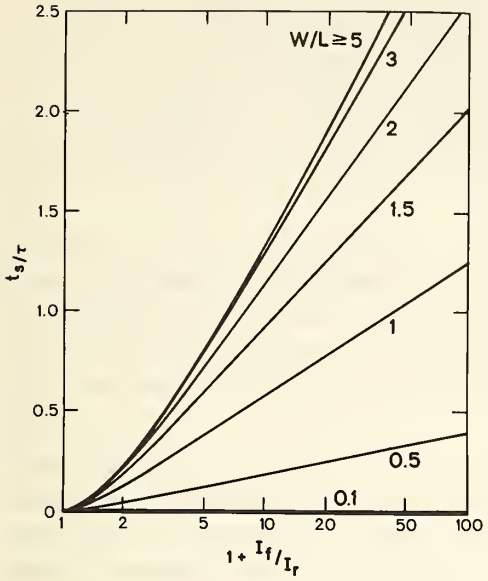


Figure 1. Diode storage time (t_s) normalized to lifetime (τ) as a function of forward-to-reverse current ratio (I_f/I_r). (The value of base width (W) normalized to diffusion length (L) is given for each curve.)

$$\sum_{m=0}^{\infty} \frac{\exp\left\{-\left[1+\left(m+\frac{1}{2}\right)^2\left(\pi\frac{L}{W}\right)^2\right]\frac{t_s}{\tau}\right\}}{1+\left(m+\frac{1}{2}\right)^2\left(\pi\frac{L}{W}\right)^2} = \left[1+\frac{I_f}{I_r}\right]^{-1} \frac{\frac{W}{L}\tanh\frac{W}{L}}{2}, \qquad (2)$$

where L is the diffusion length, is plotted in figure 1 for various values of the ratio W/L.

For $W/L \geq 5$, the exact series solution reduces to the familiar closed relation [2]:

$$\operatorname{erf}\sqrt{t_s/\tau} = [1 + I_r/I_f]^{-1}. \qquad (3)$$

For $W/L < 5$ and for sufficiently large I_f/I_r ratios, the exact solution has the form:

$$\frac{t_s}{\tau} \propto \ln\left[A\left(1+\frac{I_f}{I_r}\right)\right], \qquad (4)$$

where A is a constant which serves merely to displace the line along the horizontal axis of figure 1. The linear region extends to lower I_f/I_r ratios as the ratio W/L decreases; in the limit $W \ll L$ [3], eq (4) becomes:

$$\frac{t_s}{\tau} = \left(\frac{W}{L}\,\frac{2}{\pi}\right)^2 \ln\left[\frac{8}{\pi^2}\left(1+\frac{I_f}{I_r}\right)\right]. \qquad (5)$$

The experimental verification of eqs (3) and (4) for long and short base diodes has been reported previously (NBS Tech. Note 743, pp. 11-12).

The calculations show that for $W/L > 3$ and for $I_f/I_r < 10$ the error incurred by using eq (3) to calculate the lifetime rather than the exact solution in eq (2) is less than 2.5 percent; thus, in many cases the effects of finite base width can be ignored. The change in the functional dependence of t_s/τ on I_f/I_r, which is most easily observed as a deviation from the error function relationship, serves as a useful indicator which shows when it is necessary to correct for effects which are due to diode base width.

Initial investigation of the open circuit voltage decay (OCVD) in thin diodes based on the analysis of Choo and Mazur [4] and on experimental observations suggests that the decay transient is essentially linear in both long and short base diodes. Thus it is not possible to tell from experimental data when the result is influenced by base width considerations, and the interpretation of the OCVD transient may be ambiguous. (D. C. Lewis)

Surface Photovoltage Method — As part of the study of the recombination characteristics of the gold donor, surface photovoltage (SPV) measurements were repeated on Hall bars cut from 0.08-, 0.5-, and 1-Ω·cm, *p*-type, gold-diffused silicon wafers initially measured several months earlier. The results of these measurements suggest that increased control over experimental conditions is necessary to achieve values for the carrier diffusion length reproducible to better than 1 to 2 μm. This reproducibility is essential for useful measurements of diffusion lengths in the range 2 to 10 μm. (W. R. Thurber and A. W. Stallings)

Heat Treatment — Two additional heat treatment experiments were carried out as part of the continuing investigation of the effects of thermal cycling during the diffusion steps necessary to prepare specimens for the C-V and gold-doped silicon experiments. The objective of one of these experiments was to determine whether changes in resistivity caused by the heating experienced during diffusion could account for all or part of the discrepancy which is observed between four-probe and capacitance-voltage (C-V) resistivity measurements. Fourteen *n*-type silicon slices having nominal resistivity in the range 0.2 to 30 Ω·cm were heat treated for 2 h at 1030°C in an atmosphere of 1 percent oxygen in dry nitrogen. This cycle is the same as that used for the boron diffusion with which the junctions are formed in the diodes used for C-V measurements. Resistivity was measured by the four-probe method at the center of each slice before and after the heat treatment. The results, listed in table 2, suggest that, particularly for the higher resistivity specimens, the four-probe measurement with which the C-V measurement is to be compared should be made on slices after thermal cycling.

(R. L. Mattis, M. Cosman, D. R. Ricks, T. F. Leedy, and P. M. Sandow)

The purpose of the second experiment was to determine whether the electrical properties of gold diffused samples are influenced by heat treatments. During this

Table 2 — Effect of Heat Treatment at 1030°C for 2 h on Resistivity of Silicon Wafers

Nominal ρ (Ω·cm)	Slice No.	Resistivity (Ω·cm)		Percent Increase
		Before	After	
30	7	34.9	42.2	21.
30	8	33.2	37.2	12.
30	9	30.7	35.4	15.
30	10	30.2	31.5	4.3
8	4	7.7	7.6	- 1.3
8	12	7.8	7.9	1.3
4	10	4.06	3.93	- 3.2
4	11	3.99	4.07	2.0
3	1	3.24	3.30	1.9
1.5	7	1.76	1.76	0.0
1.5	9	1.41	1.50	6.4
1.5	11	1.37	1.38	0.7
0.2	6	0.211	0.210	- 0.5
0.2	9	0.201	0.200	- 0.5

quarter additional electrical measurements were made on the specimens heat treated previously (NBS Tech. Note 743, p. 15), for times, temperatures, and ambients similar to gold diffusions, in a new quartz tube prior to its use for gold diffusion. The results generally confirm the previous observation that small concentrations of donors were added during the heat treatment. There were, however, some anomalies in the *n*-type specimens, and further study and analysis are required to establish the nature of the added donors. (W. R. Thurber)

Plans: Study of the reverse recovery and OCVD methods will continue in order to identify the important experimental parameters and to relate these lifetime measurements to mathematical models. SPV measurements will continue on *p*-type silicon specimens and will be started on *n*-type silicon slices which were diffused with gold this quarter. Thermally stimulated measurements for characterizing GRT centers will be initiated. This includes the construction of cryostats, development of a planar test mask set, and the acquisition of equipment.

3.3. GOLD-DOPED SILICON

Objective: To characterize *n*- and *p*-type gold-doped silicon in order to develop an energy level model to predict the resistivity of silicon as a function of gold density and to provide inputs for a lifetime model.

Progress: The activation energy of the gold donor in silicon has been obtained from the results of measurements of the Hall coefficient over the temperature range 140 to 320 K on silicon wafers doped with boron and gold. Three wafers with initial resistivity of 20 Ω·cm were diffused with gold to obtain gold densities of 3.9×10^{15}, 3.1×10^{16}, and 9.9×10^{16} cm^{-3}, as determined by neutron activation analysis. After diffusion, both faces were lapped to a depth of 125 μm to remove excess gold, Hall bars were cut out ultrasonically, and aluminum contact pads were evaporated onto the side arms and end contacts.

Activation energies of the gold donor were obtained from the curves shown in figure 2 by means of a least-squares analysis [1] for the slopes. These curves are linear over most of the temperature range; points outside the linear region, indicated by squares in figure 2, were excluded from the analysis. The calculated values, listed in table 3, represent the value of the energy difference between the valence band edge and the gold donor linearly extrapolated from the temperature of the measurements to zero kelvin. The range indicated for each value of the energy is the square root of the estimated variance of the slope. The origins and significance of the small differences in energy observed have not yet been established.

A similar value was also found from Hall effect measurements made on a boron-doped wafer with initial resistivity of 1100 Ω·cm diffused with gold to a density of 1.1×10^{17} cm^{-3}. Subsequently, this specimen was annealed at 600°C for 1 h in a helium atmoshpere to expose the gold-coupled acceptor level [2] in preparation for measuring the activation energy of this shallow level. After annealing, the room temperature resistivity dropped from 1600 to 14 Ω·cm, which is consistent with a shallow acceptor density of about 9×10^{14} cm^{-3}.

(W. R. Thurber, A. W. Stallings, W. M. Bullis, and M. G. Buehler)

Plans: Hall effect and resistivity measurements as a function of temperature will continue. Electrical measurements will be made on Hall bars cut from wafers phosphorus-doped silicon with initial resistivity of 0.3 and 1 Ω·cm, which were diffused with gold this period. Discs for determination of gold density by activation analysis will also be machined from each wafer. Photoconductivity scans and spreading resistance profiles will be obtained on selected silicon wafers to study the lateral uniformity of the gold diffusion as reflected in resistivity variations.

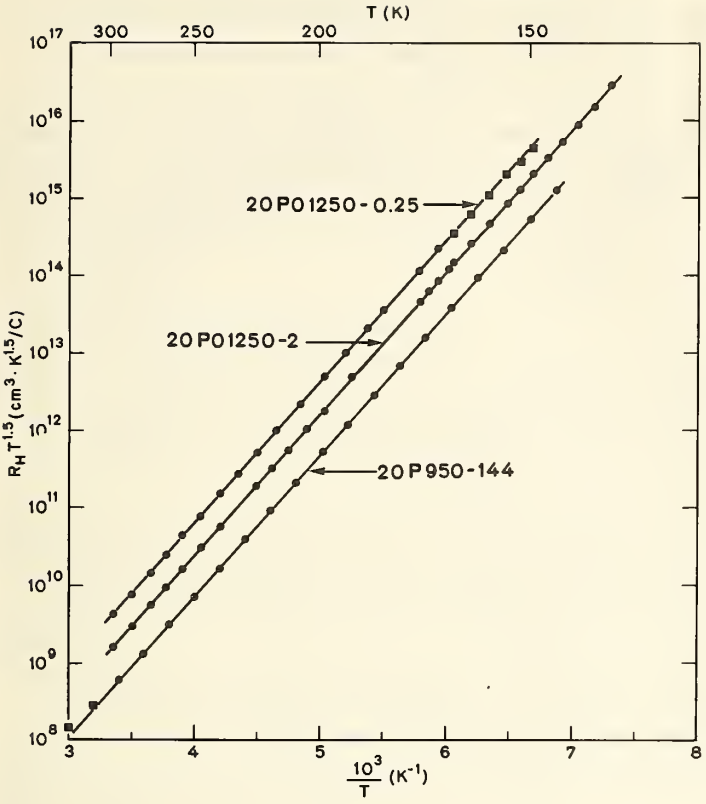


Figure 2. Activation energy plot for the gold donor in *p*-type silicon, based on Hall coefficient data. (The ordinate is the product of the Hall coefficient and the three-halves power of the temperature ($R_H T^{3/2}$) and the abscissa is inverse temperature (1000/T). The activation energy was determined from the linear region of each curve indicated by circles; non-linear portions, indicated by squares, were excluded from the analysis. Absolute temperature (T) is indicated on the upper scale.)

Table 3 — Experimentally Determined Values of the Gold Donor Energy Level

Specimen No.	Initial Resistivity (Ω·cm)	Gold Density (cm^{-3})	Energy Above Valence Band Edge (eV)
20 P950-144	20	3.9×10^{15}	0.3609 ± 0.0003
20 P01250-0.25	20	3.1×10^{16}	0.3620 ± 0.0003
20 P01250-2	20	9.9×10^{16}	0.3613 ± 0.0003
1100 P1250-8	1100	1.1×10^{17}	0.3627 ± 0.0003

3.4. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

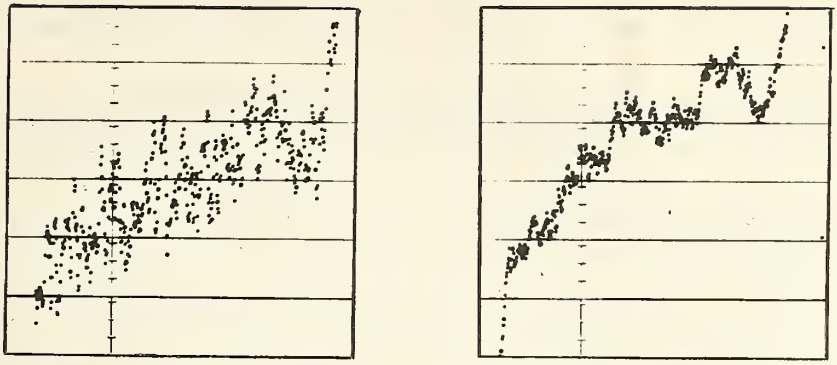
Progress: The infrared response (IRR) spectra of eight lithium-drifted germanium gamma-ray detectors were measured and identification was made of which of the five IRR spectrum groups (NBS Tech. Note 733, pp. 17-21) they correspond. Further analysis of this body of spectra has been deferred while a search of the pertinent literature to aid such an analysis is being carried out.

The germanium specimens collected for this study comprise crystals which, for the most part, had been rejected for use in the fabrication of high quality lithium-drifted gamma-ray detectors. Fortunately, the IRR technique can be applied to diodes that have poor current-voltage characteristics, as spectra can be obtained with no bias applied to the device. However, some specimens yield diodes that are so noisy that a single IRR spectrum yields no useful information; energy levels and spectrum type cannot be identified. An example of such a spectrum obtained from diode NBS-85 is shown in figure 3a. Since the noise arises from random processes, the effects of the noise are reduced if the spectrum is repeated several times and summed. The digital recording system (NBS Tech. Notes 702, pp. 12-13, and 717, p. 15) provides a convenient means for storing and summing repeated measurements. An example of the improvement achieved from ten repetitions is shown by the spectrum in figure 3b, also obtained from diode NBS-85. Both the spectrum type and the energies of the various spectral features can be identified from this spectrum.

(H. E. Dyson, W. J. Keery, and A. H. Sher)

Efforts to extend the use of the IRR technique to commercial small-volume semiconductor devices continued. Previous attempts to measure the IRR of a germanium alloy transistor (NBS Tech. Note 598, p. 16) and a silicon mesa diode (NBS Tech. Note 702, p. 13), were hampered by poor signal-to-noise ratio. Only the bandedge peak could be seen in these measurements which were carried out at 100 K. This quarter, spectra with substantially improved signal-to-noise ratios were obtained at room temperature on two 50-W zener diodes and on the previously studied silicon mesa diode. The zener diodes were commercial devices manufactured by two different companies. Each device was decapped and part of the top contact was filed away to expose as much of the silicon chip, which was approximately 2.5 mm in diameter, to the incident radiation as possible. The mesa diode chip was approximately 0.94 mm square and was bonded to an uncapped TO-5 header.

The peak previously associated only with the bandedge response was found to be broadened toward lower energies, possibly reflecting the presence of shallow dopants.



a. Single run. b. Integrated result of 10 runs.

Figure 3. Infrared response spectra obtained from lithium-drifted germanium detector NBS-85 using the digital recording system.

In one specimen, some indication was seen of a spectral feature at about 1.00 eV corresponding to that previously seen in radiation detector structures. The magnitude of the signal in the vicinity of this feature was about 1/40th that of the bandedge peak.

The improved signal-to-noise ratio was achieved by carefully aligning the device under test with the infrared beam from the monochromator; further increases in signal level were observed by focusing the incident radiation on the device. Sources of more efficient optical components are being sought. It is expected that additional spectral features can be brought out by increasing the intensity of the radiation still further. (W. J. Keery and A. H. Sher)

Plans: The studies of IRR on germanium and silicon diodes will continue. The factors affecting the performance and IRR spectra of the germanium diodes that fall into spectral types (2) and (5), characteristic of hole and electron trapping, respectively will be pursued. Further IRR measurements will be performed on small-volume silicon devices.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in mesa diodes (NBS Tech. Note 727, pp. 22-29) was postponed pending receipt of a tape for the revised TRUMP computer thermal analysis program [1]. An arrangement has been made with the author of the computer program to get a copy of the tape. Cards were generated to convert the tape for use on the NBS computer after it is received.

(C. D. Kolstad and W. E. Phillips)

The fabrication of new test circuits (NBS Tech. Note 743, pp. 23-24) to measure transient thermal response of *p-n-p*, *n-p-n*, and diode-connected transistors was completed. Measurements of thermal response were made at a case temperature of 25°C on a number of diode-connected transistors, rated at 1.8 W and encased in TO-18 cans. Because of problems with the die adhesion in many of this group of transistors the junction-to-case thermal resistance ranged from approximately 100 to 450°C/W. For this particular device type a heating power pulse width of approximately 100 ms was found to provide the maximum sensitivity to voids. It was found that in the devices with higher thermal resistance the change in junction voltage during heating was significant for heating currents selected to obtain a measurable response in devices with lower thermal resistance. Consequently, the simplifying assumption of constant power dissipation that was found to apply in previous thermal response measurements (NBS Tech. Note 727, pp. 27-29) did not apply in this case. Nevertheless the thermal response was a satisfactory measure in locating devices with voids. This heating voltage change with temperature is not a problem when measuring the device connected as a transistor if the option of using a relatively high collector voltage is used. Then, the decrease in the emitter-base voltage due to heating is small compared to the total emitter-collector voltage. (F. F. Oettinger and R. L. Gladhill)

Specimens were prepared for an experimental study of the relationship between thermal response and voids in transistor die attachment. Three groups of 10 *n-p-n* silicon power transistor chips, 35 mils (0.89 mm) square, were bonded to standard, gold-plated, iron-nickel-cobalt alloy, glass-backed TO-5 headers with 15-, 20-, or 25-mil (0.38-, 0.51-, or 0.64-mm) diameter dimples ultrasonically machined into the bonding surface to produce voids that are approximately 15, 25, or 40 percent of

the total chip bonding area, respectively. Ten control devices were bonded without voids at the same time as each group of 10 devices was bonded with a given size void. (T. F. Leedy and P. M. Sandow)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes previously investigated will continue after the revised TRUMP thermal analysis program is received and suitably modified for use on the NBS computer. A heat sink will be fabricated for use in infrared microradiometer measurements of the previously investigated diodes with controlled voids to compare the actual peak junction temperature with the measured steady-state thermal response. After checkout of the circuitry for measuring transient thermal response of *n-p-n* transistors, measurements will be made on the transistors with controlled voids in both the transistor and diode-connected transistor operating modes for evaluation of the die adhesion.

4.2. WIRE BOND EVALUATION

Objective: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices and, where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progress: Measurements of pull strength of unannealed and annealed aluminum wire bonds as a function of pull rate continued, but the analysis is not yet complete. Experimental study of factors affecting the pull test on two-level bonds was begun. Work on the fabrication of aluminum balls for bonding was resumed. A report summarizing the work on ribbon wire is being prepared. The preparation of an annotated bibliography of limited distribution reports on bonding continued.

Ribbon-Wire Bonding — Implementation of ribbon-wire bonding has begun in some military laboratories as a result of the NBS study of this technology. A considerable amount of time has been spent in consultation with laboratories that purchased ribbon-wire clamps for modifying round-wire bonding machines. One laboratory was visited to advise personnel on the setting up of bonding equipment for use with ribbon wire. During the course of continuing ribbon-wire research, modifications were made to a ribbon-wire clamp manufactured for use on a commercial round-wire bonding machine to decrease damage to the wire during the bonding operation. (H. K. Kessler)

Aluminum Ball Formation — Work resumed on the formation of balls on fine aluminum (1% silicon) wire to facilitate ultrasonic ball bonding of aluminum wire (NBS Tech. Notes 495, p. 30, and 520, p. 43). A stream of gas heated to about 900°C was used in an attempt to make the balls; however, the gas flow rate necessary to produce melting was also sufficient to blow off the fused portion of the wire. Although

some equipment modifications might be made to reduce the flow rate and thus minimize the blow off, it was decided to return to a method described earlier (NBS Tech. Note 495, p. 30) in which a capacitor discharge supplies the energy to fuse the wire.

With a section of the aluminum wire grounded, the cut end is brought in contact with a platinum electrode, discharging the capacitor. This technique often formed acceptable balls, even in a normal room air ambient. However, in some cases the ball fused to the electrode. To avoid this, the wire was moved several thousandths of an inch away from the platinum electrode, and the air gap was broken down by discharge of a trigger transformer of the type used in photographic electronic flash units. Energy for fusion was still supplied by the capacitor discharge. The size of the aluminum ball thus formed was found to be dependent upon the capacitor discharge rate. At present, aluminum (1% silicon) wire yields spherical balls with diameter 2 to 3 times that of the wire about 30 to 40 percent of the time; in limited experiments with gold wire, a ball yield of 50 to 60 percent was obtained. (H. K. Kessler)

Pull Test Evaluation — Work was begun to investigate the effects of the variables that affect the measured pull strength of bonds made on two-level substrates. Bonding pads were fabricated as previously described for the single-level work (NBS Tech. Note 527, pp. 39-40); the aluminum was sintered by heating the wafer to 550°C in helium for 15 min. Strips of silicon 0.05 in. (1.3 mm) wide, obtained by scribing and breaking a prepared substrate, were affixed with a high temperature glue to another substrate so that the bonding pad arrays lined up as shown in figure 4. Thus two-level substrates were obtained with rows of bonding pads raised by the thickness of the silicon strip (about 0.25 mm) above the bonding pads on the base substrate. It was necessary to position the silicon strip carefully on the base substrate so that a constant spacing between the upper pad and the lower pad was maintained along the length of the strip.

Figure 5 shows the geometric variables for the double-bond pull test on the two-level substrates [1]. In the experiments to be described, the values of the geometric variables were as follows: $d = 1.0$ mm, $\alpha = 0.5$, $\phi = 0$, $H = 0.25$ mm. The nominal pull angle, β, was about ±15 deg. For the two-level bond, the difference between the angles β and ϕ in the plane of the bond loop must be taken into account since the normal to the substrate is no longer in the same direction as the normal to the line joining the bonds. The angle β is defined as that formed between the direction of pulling force and the normal to the lines joining the bond terminals (positive in the direction toward the second bond). The angle ϕ is that angle formed between the direction of pulling force and the normal to the substrate (positive in the direction toward the lower bond). The relationship between the two angles is $\phi = \pm(\beta - \beta_0)$ where the positive sign obtains if the first bond is the higher (in which case β_0, the angle between the substrate and the line joining the bond terminals

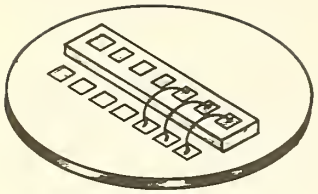

Figure 4. Pictorial illustration of two-level substrate.

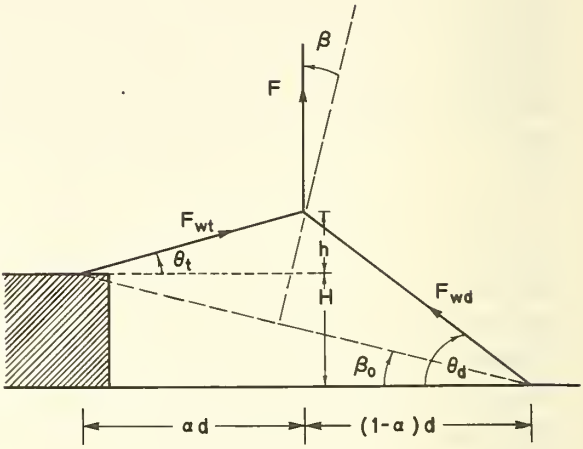

Figure 5. Geometric variables for the pull test for bonds made on two-level substrates for pulling normal to the substrate. (For this case, the angle ϕ between the normal to the substrate and the pulling direction is zero. The distance d is the total bond-to-bond spacing in the plane of the substrate.)

is negative), and the negative sign obtains if the first bond is the lower (in which case β_0 is positive).

At a fixed loop height (h) of about 0.15 mm, seven power series were run with tool tip displacements from about 0.75 to 2 μm peak-to-peak. The pull strengths of groups of 10 bonds made at each value of tool-tip displacement were measured. The resulting curves of pull strength as a function of displacement were similar in shape to those generated previously for single-level substrates (NBS Tech. Note 560, pp. 30-33), and the variability in mean pull strength for groups of 10 bonds appeared to be about the same for the two-level measurements as for the single-level ones.

Initial experiments were performed in which the variation in pull strength as a function of loop height (h) was examined. Groups of 10 bonds were made at seven different loop heights. Tool-tip displacement was approximately 1 μm peak-to-peak and bonding force was 25 gf (24.5 mN). This was done both for the first bond made on the high pad and for the first bond made on the low pad. In all cases failure occurred at the heel of the first bond. The measured pull strengths are plotted

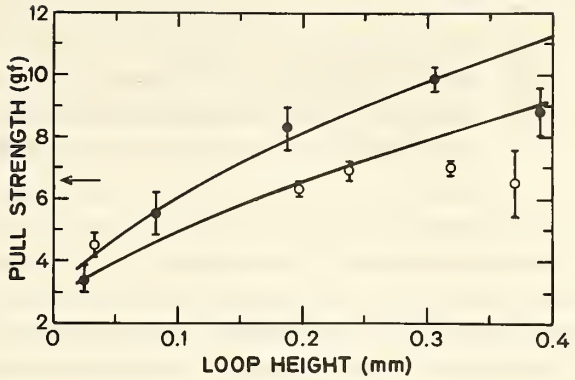

Figure 6. Pull strength of unannealed, round-wire, two-level bonds as a function of loop height. (Solid points are for the first bond made on the high pad; open points are for the first bond made on the low pad. The data points represent the mean of 10 bonds, all of which ruptured at the heel of the first bond. Error bars indicate one sample standard deviation above and below the mean. The solid curves were calculated by resolution of forces using the wire tensile strength indicated by the arrow.)

against loop height in figure 6 for both cases (solid points - first bond high, open points - first bond low). The plotted points represent the mean value of the 10 bond pulls and the error bars indicate one sample standard deviation on either side of the mean. The solid lines represent the values predicted by a resolution of the forces for each case [2]. The agreement between the trend of the theoretical curve and that of the experimental points for the first bond made to the high pad appears to be good for loop heights less than about 0.3 mm. For higher loops, the apparent pull strength is reduced as previously observed for both single-level round- and ribbon-wire bonds (NBS Tech. Note 743, pp. 29-31). The agreement between the theoretical prediction of measured pull strength as a function of loop height and the experimentally determined values does not appear to be as satisfactory for the experiment where the first bond was made on the low pad.

The results for the case of the first bond made on the low pad generally show overall pull strengths less for a given loop height than those for the first bond made on the high pad. This is in agreement with the experimental measurement of the effects of angle β (NBS Tech. Note 727, pp. 41-43) in which higher pull strengths were observed for negative values of the pull angle β than for positive values.

(K. O. Leedy, C. A. Main, and A. H. Sher)

Bibliography and Critical Review — The comprehensive review of wire bond fabrication and evaluation (NBS Tech. Note 743, p. 31) has been published [3] and initial distribution was completed. Copies are available on request to the author. The preparation of the annotated bibliography of limited distribution reports continued. About 90 reports have thus far been assigned key words and given annotations. About 110 reports in all are expected to be compiled in the bibliography.

(H. A. Schafft)

Plans: Experimental study of the pull test on two-level substrates will continue; effects of position of the pulling hook on pull strength will be determined, the results of varying the bond pull angle α (NBS Tech. Note 743, pp. 27-28) will be examined, and measurements of pull strength as a function of loop height will be repeated. Further measurements of pull strength for annealed wire bonds as a function of pull rate and bond angle will be carried out in the continuing search for the causes for the apparent lack of agreement between the measured pull strength values and the resulution-of-forces calculation. The report summarizing the ribbon-wire bonding work will be completed. Work on a report summarizing the effects of various parameters affecting the pull test will begin.

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5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Measurements made on a variety of different types of power transistors to compare the emitter-only switching technique with the emitter-and-collector switching technique confirmed that the emitter-only switching technique is the preferred method for measuring thermal resistance of power transistors. The investigation of several unusual observations made on devices susceptible to severe current constrictions continued with consideration of their effect on the screen for hot spots based on measurement of common-emitter current gain.

Standardization Activities — The devices for the preliminary round-robin experiment on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors have been measured by the sixth participant. Based on an initial review of the results to date, the committee has concluded that a revision of RS-313-A, EIA-NEMA Standard on Thermal Resistance Measurements on Conduction Cooled Power Transistors, is in order.

Work on proposed revisions of Method 1012, Thermal Characteristics, of MIL-STD-883, Test Methods for Microcircuits, undertaken at the request of the cognizant agency, continued. (F. F. Oettinger and S. Rubin)

Thermal Resistance Methods — Preliminary emitter-only switching measurements of transistor thermal resistance (NBS Tech. Note 743, pp. 34-35) indicated the usefulness of this method, but they revealed the existance of an excessively long electrical transient after turn off in relatively wide base transistors, because of the slow response of the diode in series with the emitter. The problem was solved by adding a switching transistor in series with the diode switch. Subsequent tests showed that the series switching transistor was adequate to handle the switching by itself; consequently, in all the tests reported this quarter switching was done only with a series transistor in the emitter lead.

To provide a broader basis for conclusions regarding the emitter-only switching technique, 18 transistors representing 11 transistor types which differed in registration number, manufacturer, or fabrication technology were selected for test. Several different fabrication technologies, including single diffused, epitaxial base, and triple diffused were represented. Base widths ranged from approximately 2.5 to 25 μm. The rated power dissipation was in the range 20 to 35 W; all devices were encased in TO-66 cans. Tests were made with test currents of 6.5 and 32 mA, a heating current

of 1 A and a collector-emitter voltage of 20 V. Three 20-W units were also measured with a heating current of 500 mA. Tests were run on all 18 transistors using both emitter-only and emitter-and-collector switching. The results confirmed the observation made in the preliminary investigation that the emitter-only switching method of thermal resistance measurement consistently yields a value indicative of a higher apparent junction temperature, which more nearly approaches the peak junction temperature, than does the collector-and-emitter switching method for the same delay time after the cessation of the power pulse.

The initial experiments using emitter-only switching also suggested that for a given fixed test current the constant of proportionality between base-emitter voltage and the junction temperature is relatively unaffected by the magnitude of the collector-emitter voltage applied during calibration. The present test results confirmed this initial indication. With the exception of one transistor which appeared to develop a surface contamination problem during the testing, the change in the value of the proportionality constant was negligibly small when the collector-emitter voltage was changed from 2 to 10 V for a test current of 6.5 mA. Greater changes were observed for a test current of 32 mA when the collector-emitter voltage was increased from 2 V to the highest value appropriate to the particular transistor. The increase in this case was 2.5 ± 1.7 percent.*

In addition to the variation of the proportionality constant with collector-emitter voltage, data from the tests indicated the variability from device to device, as summarized in table 4. The variation is less for calibration with voltage on the collector, as used for testing with emitter-only switching, than it is for calibration with the collector open, as is the case for testing with emitter-and-collector switching. This is an important consideration if commercial tests are to be made without the need to calibrate each individual device of a lot. In each case where two transistors of the same type were tested, the difference in the proportionality constants for a given test current was always less than 3 percent of the mean value. In two cases, transistors of similar registration number and fabrication technology made by two different manufacturers were studied. In these two groups, the largest spread was also less than 3 percent of the mean. Even on the basis of these limited results, it would appear that for a given lot from a given manufacturer, the variation in proportionality constant would generally be small enough to allow the use of a single value for the entire lot.

The effect of test current magnitude on the measured thermal resistance of devices operating in the non-constricted mode was further investigated. It was observed that the larger the test current magnitude, the shorter the decay time for electrical

* mean value ± one sample standard deviation.

Table 4 — Proportionality Constant Between Base-Emitter Voltage and Junction Temperature for Seventeen Medium Power Transistors of Ten Different Types

Switching Mode	Emitter-Collector Voltage (V)	Test Current (mA)	Mean Value (mV/°C)	Relative Sample Standard Deviation (%)
Emitter-only	2.	6.5	2.28	3.41
Emitter-only	2.	32.	2.12	2.71
Emitter-and-Collector	0.	6.5	1.97	4.63
Emitter-and-Collector	0.	32.	1.78	4.76

transients, but that after the electrical transients no longer interfered, the measured thermal resistance did not depend strongly on the test current magnitude. Because of the different response of the transistors under test, the time interval after the cessation of the power pulse required for the decay of electrical transients was different for different transistor types. For most of the transistors tested, a delay time of 20 μs was adequate to assure a change of less than 1 percent in measured thermal resistance when the test current was changed from 6.5 to 32 mA, but for four very slow, single-diffused transistors a delay time of 100 μs was required. Previous observations suggest that the test current magnitude may have greater effect when measuring thermal resistance in the presence of severe current constrictions.

During the tests described above it was observed that positive voltage transients of large magnitude appeared between the emitter and base of the single-diffused transistors chosen for test when switching from the heating to the testing portions of the cycle. It was further noted that the peak magnitude of this excursion was the same as the collector-base voltage unless the collector-base voltage was greater than the reverse-bias breakdown voltage of the emitter-base junction. This suggested that a reverse bias breakdown was occurring across the emitter-base junction of these transistors. This breakdown, which was observed only in transistors where the speed of the transistor is less than the switching speed of the switching transistor in the emitter circuit, can be prevented by connecting a zener diode and fast-recovery diode back to back between the emitter and base of the transistor. The fast-recovery diode is connected to the base in a blocking configuration when the emitter base junction is forward biased. The zener diode, which has a breakdown voltage 1 or 2 V below that of the emitter-base junction of the transistor under test, is connected so that it breaks down when the emitter-base junction is reverse biased.

(S. Rubin and F. F. Oettinger)

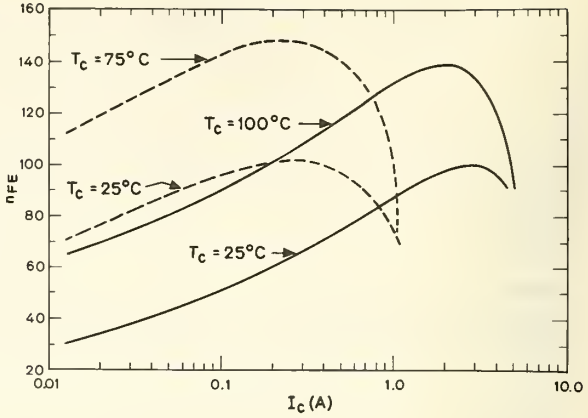


Figure 7. Common-emitter current gain (h_{FE}) as a function of collector current (I_c) at two case temperatures (T_c) for a power transistor which shows an abrupt decrease in h_{FE} on formation of a hot spot (dashed curves) and a power transistor which shows an abrupt increase in h_{FE} on formation of a hot spot (solid curves). (Collector-emitter voltage was 70 V for the former and 10 V for the latter.)

Screen for Hot Spots — Some unusual effects have been observed on several devices which are susceptible to severe current constrictions. At least two devices have been observed for which the common emitter current gain (h_{FE}) abruptly increased when the severe current constriction occurred. This change in h_{FE} is opposite to the change that has generally been observed for most other devices when a current constriction occurs (NBS Tech. Note 560, p. 41). Distinct differences were found in the dependence of h_{FE} on collector current (I_C) for the two types of devices. Measurements of h_{FE} were made as a function of I_C for two values of case temperature on devices which showed both types of change. Typical curves are shown in figure 7. The maximum in h_{FE} occurs at much higher currents for the device in which h_{FE} increases abruptly on formation of a hot spot due to severe current constriction than for the more usual devices. Even though the collector-emitter voltage (V_{CE}) used in generating the curves shown in figure 7 is considerably lower than the value at which the hot spot forms, it is thought probable that differences in the h_{FE} - I_C characteristic may account for the different behavior of h_{FE} on hot spot formation.

A second observation was that in some cases hot spots jump from one location to another or become unstable as V_{CE} is decreased [1]. In some devices of one particular type it was observed that as V_{CE} was decreased, the initial hot spot jumped to another location where a stable current constriction occurred, while other devices of the same type became unstable in the hot-spot mode and went into second breakdown as V_{CE} was decreased. The fact that a device may go into second breakdown in the hot-spot mode as the power is decreased may be an important consideration when one is screening devices for second breakdown.

In a third test, it was found that although a device formed a stable current constriction for a range of collector currents and collector voltages when the case

temperature was 25°C, a stable constriction was no longer formed at a case temperature of 50°C. Instead, the device went into second breakdown at the same values of current and voltage that stable constrictions were formed at the lower case temperature. This observation suggests that although the formation of a current constriction appears to be nearly independent of the temperature of the device (NBS Tech. Note 592, pp. 49-51), the mechanism of current constriction stabilization may be temperature dependent. Thus, it may be necessary to maintain the device case temperature at a specified value when using the screen for hot spots to avoid such instabilities. (D. L. Blackburn and F. F. Oettinger)

Plans: Work on standardization activities related to thermal measurements will continue. The proposed revisions of Method 1012 of MIL-STD-883 will be completed. Measurements of peak junction temperature, using an infrared microradiometer, will be made on the transistors that were tested for thermal resistance this quarter. An investigation into the mechanism of the emitter-base voltage transient which occurs when switching the emitter with a series transistor during emitter-only thermal resistance measurements will be completed.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: The study of the reproducibility of the conversion loss measurement continued, but measurements were interrupted by erratic operation of the modulation attenuator, which required extensive repairs. Standard deviations were calculated for all recent measurement runs, and the application of statistical control charts to these measurements was started. An important equation relating conversion loss measurement uncertainty to modulation attenuation uncertainty was derived and tabulated. A comprehensive report on work to date has been started.

Based upon the 24-h measurement runs previously reported, one apparently stable diode was selected for measurement over a one-week period without being removed from the holder. These measurements were considered as constituting a single run and compared with three previous 24-h runs (the diode having been ejected and reinserted between the first and second runs and between the third and fourth runs). The results of the measurements made under standard conditions (NBS Tech. Note 743, p. 38) are summarized in table 5.

A series of control charts [1] was prepared for this diode using various groupings of the data. These charts were reasonably consistent in showing that while the

Table 5 — Repetitive Conversion Loss Measurements on a Single Diode

Run No.	Mean Value (dB)	Sample Standard Deviation (dB)	Relative Sample Standard Deviation (%)
1	4.394	0.021	0.48
2	4.373	0.019	0.43
3	4.372	0.012	0.27
4	4.370	0.018	0.41

standard deviations were in control, the means were not; the observed monotonic decrease of 0.024 dB resulted in subgroup points which extended beyond the control lines.

The sample standard deviations for all runs with all diodes ranged from 0.006 to 0.066 dB (0.13 to 1.5%) with an average of 0.023 dB (0.48%). All of these figures are based upon all data taken under standard conditions for each run. Except in one instance, diodes for which more than one run was taken showed little change in the mean value of the conversion loss on being remeasured after removal and reinsertion. This suggests that the diode-to-holder contact may be less of a problem than had been originally thought, although it is certainly of significance.

(S. Eshleman, F. H. Brewer, and J. M. Kenney)

It was intended that many more measurements would be made on the diode selected for long-term study, but it was found that variations in the force used to turn the modified rotary-vane attenuator, used as the mechanical modulator, against the stops resulted in variations in r-f power and mixer output voltage. Disassembly of the attenuator revealed poorly fitted main bearings, which may have loosened sufficiently to allow unwanted motion of the center section as it was forced against the stops.

All critical bearing-alignment surfaces on the attenuator were re-machined, and the bearings proper were either replaced or rebuilt and then lapped in place after assembly. Only very limited electrical testing has been performed following the repairs, but the reproducibility of the attenuation seems to be markedly improved.

(L. M. Smith and J. M. Kenney)

In order to assess the significance of error in the modulation attenuator as to both reproducibility and systematic uncertainty, the sensitivity of conversion loss to attenuation used to obtain the modulation increment was determined. The basic conversion loss equation for the voltage form of the incremental modulation method is:

$$L_M = \frac{8m^2PR}{V^2M}\ , \tag{6}$$

where L_M is the conversion loss (power ratio), m is the modulation factor (voltage ratio), P is the unmodulated local oscillator power (watts) available to the mixer, R is the incremental (i-f) load resistance (ohms), V is the incremental (i-f) load voltage (volts), and M is the i-f mismatch factor (power ratio). The conversion loss may be expressed in terms of attenuation by using the relationship between attenuation and modulation factor:

$$L_A = [(1 + m)/(1 - m)]^2, \tag{7}$$

where L_A is the attenuation (power ratio).

By expressing both conversion loss and attenuation in decibels ($L_M' = 10 \log L_M$ and $L_A' = 10 \log L_A$) one can obtain the desired sensitivity:

$$\frac{\partial L_M'}{\partial L_A'} = \frac{2}{10^{L_A'/20} - 10^{-L_A'/20}} . \tag{8}$$

For $L_A' << 20$, series expansion of the exponentials leads to the approximation:

$$\frac{\partial L_M'}{\partial L_A'} \approx \frac{8.686}{L_A'} \tag{8a}$$

For the 1-dB attenuation currently used, the sensitivity (using the exact expression) is 8.66673 dB/dB. Thus, for an attenuator uncertainty of ±0.001 dB, the conversion loss uncertainty is about ±0.009 dB. The 3-sigma precision of ±0.0019 dB assigned to the calibration of the 1-dB stop is thus equivalent to a loss uncertainty of about ±0.016 dB. The conservative systematic uncertainty of ±0.005 dB assigned to this calibration adds an additional ±0.043 dB, for a total attenuator contribution of about ±0.060 dB. From eq (8a) it can be seen that to halve the uncertainty from this source would require about twice the attenuation; it can be shown, however, that this would increase the equivalent signal power by about 6 dB. There is thus a trade-off between attenuator uncertainty and mixer nonlinearity, but only the former can currently be quantified. (J. M. Kenney)

Plans: First priority will be given to completion of the technical report on progress to date. The reproducibility of the modulation attenuator settings will be checked. If satisfactory, the attenuator will be recalibrated by the NBS Electromagnetics Division. This calibration will be made for several increments, the required vernier micrometer stop positions being recorded for each, thus allowing a quantitative study of mixer linearity. The precision of setting the micrometer stops will also be determined during this calibration, since this is crucial to the linearity study. Following the attenuator calibration, studies of the reproducibility of the conversion loss measurement will be resumed, using both Schottky-barrier and point-contact diodes.

5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: A large part of project activity was again devoted to assembling equipment and establishing techniques for measuring transistor high-frequency scattering parameters (S-parameters) at the wafer level. A technique for checking the phase-angle calibration of a vector voltmeter has been developed, and a method for verifying the overall operation of a delay-time system employing the vector voltmeter has been tested using R-C delay-time networks on TO-5 headers. Good agreement has been obtained between the measured and calculated electrical behavior of the R-C delay-time networks on TO-72 headers intended to be circulated as part of a forthcoming interlaboratory comparison of S-parameter measurements.

Measurement of High-Frequency Transistor Parameters at the Wafer Level — The probe restoring force and probe tip protrusions of the special probe assemblies (NBS Tech. Note 743, pp. 40-41) to be used for measuring transistor high-frequency S-parameters at the wafer level were measured. In addition the shapes of the probe tips and the extent of skidding of probes on being applied to metallized silicon with various forces were examined microscopically. Details have been provided to the sponsor for use in adjusting the probe holder to ensure adequate contact between the probe tips and the contact pads on the test wafer. (F. H. Brewer and D. E. Sawyer)

Probe reference units, for use in determining the electrical effects of the probe assembly on the S-parameter measurements, have been fabricated on alumina substrates, 1 in. (25 mm) square by 0.015 in. (0.38 mm) thick, by a sequence of masking and etching operations. As received, the substrates were coated with 6.3 μm of gold over 10 nm of chrome over tantalum nitride with nominal sheet resistivity of 40 Ω/□. A typical unit is shown in figure 8. The white background material is the bare ceramic substrate, the gray areas are the gold contact pads, and the dark regions are exposed tantalum nitride. The narrow contact stripes are 0.002 in. (0.05 mm) wide and 0.006 in. (0.15 mm) long. The U-shaped structure at the center enables the resistance between the contact pads and the resistivity film to be determined.

(T. F. Leedy, P. M. Sandow, and D. E. Sawyer)

The d-c resistance of 110 resistive elements in 22 units was measured on each of the two substrates with the previously described work station (NBS Tech. Note 743, p. 41). The average resistance of the elements measured on one wafer was 22.2 Ω. A technique for specifying the location of any resistor on the substrate was developed so that the resistance of elements to be used in future tests can be individually measured and recorded. It is estimated that individual measurements can be reproduced to better than 0.5 percent, based on several replications about 3 weeks apart.

(F. H. Brewer)

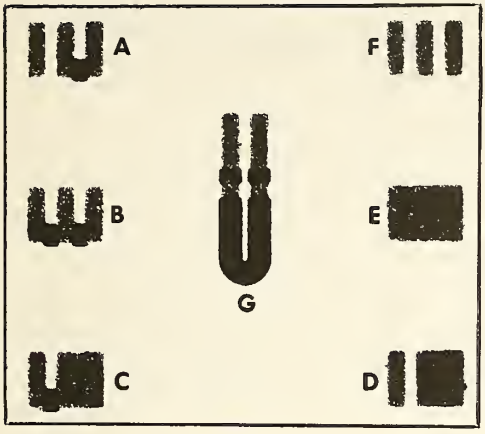


Figure 8. Probe reference unit. (Magnification ∿58 X.)
A Open - Resistor
B Resistor - Resistor
C Resistor - Short
D Open - Short
E Short - Short
F Open - Open
G Resistor Test Pattern

Vector Voltmeter Delay-Time Instrumentation — For a component or system excited by a sinusoid, an error in the measurement of the phase angle between the input and output electrical signal causes a proportional error in the phase delay time attributed to the component or system [1]. A method for determining the accuracy of the phase angle calibration of a commercial vector voltmeter was developed and tested for signal frequencies from 2.777 to 27.77 MHz over a wide range of input signal amplitudes. Intervals of 2.777 MHz were chosen for convenience, since, for the particular instrument used, the phase angle is presented in degrees, so that the relationship between the delay time (τ_{ph}) in nanoseconds and the phase angle lag (θ) in degrees is

$$\tau_{ph} = \frac{2.777\ \theta}{f} \quad , \tag{9}$$

where f is the frequency in megahertz. The block diagram of the test circuit is shown in figure 9. The circuit characteristic impedance is 50 Ω; all connections are made with coaxial cables or rigid coaxial air lines.

The calibration of the scales on the constant-impedance, variable-length, trombone lines was first checked. This was done by replacing the trombone in channel A by a convenient length of air line and connecting this trombone in series with the one in channel B. With both trombones collapsed, a sinewave signal of 400.00 MHz was applied and the vector voltmeter phase angle noted. The trombones were then varied to shift the phase by exactly 360 deg, so that the phase angle previously noted was restored. Then the sum of the incremental delay times read on the trombone scales should be equal to 2.500 ns, the reciprocal of the test frequency. Since it is only required that the phase angle indication be the same before and after the adjustment, the result is independent of the calibration of the vector voltmeter. The measurement was repeated several times for trombone line settings in the range 0.5 to 1.5 ns; the

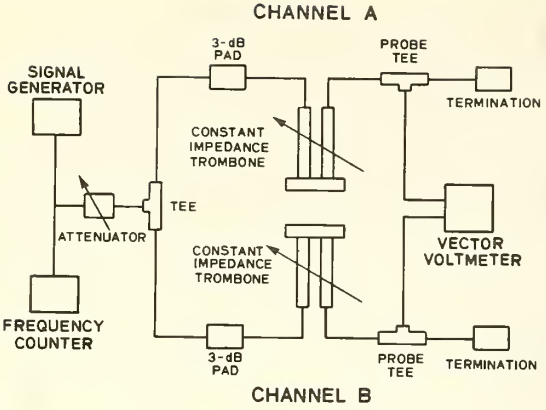
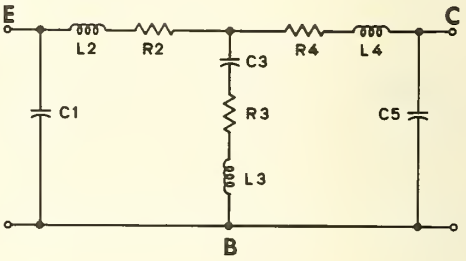


Figure 9. Circuit for phase calibration of vector voltmeter.

Figure 10. Equivalent circuit for R-C delay-time network.



total delay times measured were slightly larger than but always within 2 ps (0.1%) of the reciprocal of the test frequency.

To determine the accuracy of the vector voltmeter phase-angle calibration, a known increment of phase delay was introduced into channel B with the trombone, and the change in vector voltmeter phase angle was compared with that computed from eq (9). The results indicated that the phase angle presentation is low by about 3 percent over a wide range of signal amplitude and frequency.

After the vector voltmeter was calibrated, delay-time measurements were made on four R-C networks mounted on TO-5 headers (NBS Tech. Note 727, pp. 54, 56) with nominal delay time in the range 212 to 665 ps on a transistor delay-time measurement system similar to one described elsewhere [2] which incorporates the vector voltmeter. The equivalent circuit shown in figure 10 was assumed for the R-C networks. The known elements are R_2, R_4, and C_3; the nominal delay-time is equal to the product of R_4 and C_3. For these networks it was found experimentally that the pin-to-header capacitances C_1 and C_5, lead wire and header pin inductance L_2, and resistive losses R_3 may be neglected. At frequencies between 5 and 30 MHz, delay-times were found to

be within 10 percent of the nominal value when the measurements were corrected for the effect of a constant inductance of 4.5 nH in the complete collector-base loop. A portion of this resides in the measurement circuit outside the R-C network, while the remainder is the sum of the lead wire and header pin inductances L_3 and L_4. With the entire 45.5 nH attributed to the measurement circuit itself; one may calculate an upper bound to transistor delay-time error associated with inductance in the collector-base circuit. (D. E. Sawyer)

Interlaboratory Comparison of S-Parameter Measurements — Six laboratories have been contacted by a sponsor and have agreed to participate in an interlaboratory comparison of transistor S-parameter measurements. Minor modifications have been made in the test plan as a result of suggestions by the participants, but the general outline of the previously developed plan (NBS Tech. Note 743, pp. 42-43) has not changed.

The devices to be circulated to the participants for measurement were selected, and their characteristics were measured and recorded. Tests were also made on the R-C networks mounted on TO-72 headers, which are to be measured in the interlaboratory comparison. The various parasitic elements in the equivalent circuit of figure 10 were evaluated from S-parameter measurements made at frequencies from 100 MHz to 1 GHz with the networks mounted in appropriate transistor fixtures. The inductance of the wire bonds and header pins, represented by L_2, L_3, and L_4, typically was in the range 1 to 3 nH. The pin-to-header capacitances, represented by C_1 and C_5, were about 0.7 pF. Loss in the capacitor C_3, represented by R_3, was typically 1 to 1.5 Ω. Measurements of Z_{11} on these networks yielded values within 5 percent of the response calculated from the known values of the discrete elements R_2, R_4, and C_3 and the above values for the parasitic elements.

Preparation of computer programs for analyzing the data from the interlaboratory comparison was begun. (G. J. Rogers, F. H. Brewer, and V. A. Cevrain)

Plans: Delay time of several transistors will be measured on several types of measuring instruments, and the results will be analyzed and compared. The development of computer programs for analyzing the results of the S-parameter interlaboratory comparison will continue, and the measurement phase will be completed.

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APPENDIX A
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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Secretary, Subcommittee 91, Editorial; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections; Subcommittee 11, Quality and Hardness Assurance

J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections

J. C. French, Chairman, Subcommittee 91, Editorial; Subcommittee 11, Quality and Hardness Assurance

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Photoresist and Dielectrics Sections

D. C. Lewis, Subcommittee 11, Quality and Hardness Assurance

C. P. Marsden, Committee Secretary

R. L. Mattis, Lifetime Section

W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals; Crystal Perfection, Mechanical Properties of Semiconductor Surfaces, Compound Semiconductors; Impurities in Semiconductors, and Germanium Sections

A. H. Sher, Germanium Section

W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standards, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX C
SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Thin Metal Films (J. Krawczyk and T. F. Leedy)

Aluminum film steps of nominal 2 μm thickness on optical flats were produced for the NBS Dimensional Technology Section for use in evaluating such films for small step measurement and calibration.

Thin films of gold, nickel, or chromium were vacuum evaporated onto various polymeric films for fabrication into piezoelectric and pyroelectric detectors by the NBS Instrumentation Applications Section.

2. Channel Electron Multipliers and Proportional Counters (Y. M. Liu)*

Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center contunued. The multipliers and a flight electrostatic analyzer were calibrated in terms of plate voltage as a function of electron energy using electrons from the low energy accelerator. Rejection rate and angular distribution were also measured.

Xenon- and carbon dioxide-filled beryllium-window proportional counters intended for use in the Helios Sun Probe x-ray experiment were examined to determine their counting characteristics.

3. Electrical Burnout Studies (W. K. Croll and H. A. Schafft)†

Examination of 244 circuits on 61 quadruple two-input, positive NAND gates was completed for the Harry Diamond Laboratories to assist in establishing degradation and failure modes. A discussion of the primary failure mode observed is given in Appendix E.

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* NBS Cost Center 4254429

† NBS Cost Center 4251541

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702883
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	AD 740674
December 31, 1971	727	June, 1972	AD 744946
March 31, 1972	733	September, 1972	AD 748640
June 30, 1972	743	December, 1972	

Current Publications:

As various phases of the work are completed, publications are preapred to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author.

Schafft, H. A., Testing and Fabrication of Wire-Bond Electrical Connections — A Comprensive Survey, NBS Technical Note 726 (September, 1972).

Mattis, R. L., and Baroody, A. J., Jr., Carrier Lifetime Measurement by the Photoconductive Decay Method, NBS Tech. Note 736 (September, 1972).

Phillips, W. E., Interpretation of Steady-State Surface Photovoltage Measurements in Epitaxial Semiconductor Layers, *Solid-State Electronics* 15, 1097-1102 (October, 1972).

Sawyer, D. E., Prevalent Error Sources in Transistor Delay-Time Measurements, *IEEE Trans. Nucl. Sci.* NS-19, No. 6, 121-124 (December, 1972).

Blackburn, D. L., Schafft, H. A., and Swartzendruber, L. J., Nondestructive Photovoltaic Technique for the Measurement of Resistivity Gradients in Circular Semiconductor Wafers, *J. Electrochem. Soc.* 119, 1773-1778 (December, 1972).

APPENDIX E
BREAKDOWN TRACKS PRODUCED BY VOLTAGE TRANSIENTS

One of the primary failure modes of monolithic integrated circuits stressed with voltage transients is a breakdown track electrically shunting one or more p-n junctions* [1], [2]. These tracks are observable through an optical microscope and often appear as a localized surface irregularity across the line where the p-n junction intersects the silicon surface as shown in figure 11. This irregularity usually joins two adjacent aluminum metallization stripes connected to the underlying n- and p-type regions of the involved junctions. Sometimes, it appears that aluminum from these stripes has migrated into the breakdown track, as shown in figure 12, resulting in a pale-white smear. In some cases a junction is not involved; tracks may occur between the metallization stripes connected to the ends of a diffused resistor. In all cases the track acts electrically as a resistive path shunting the involved metallization stripes.

These breakdown tracks have been variously described and named. They have been called junction shorts [1], flash-across shorts [2], metallic bridging shorts [3], white spears [4], and surface zaps [5].

Workman [2] stated that the most frequently occurring failure mode resulting from electrical overstress in silicon monolithic microcircuits is a breakdown track which he called a flash-across short. He observed that this failure usually occurs at junctions stressed with fast-rise-time, reverse-bias voltage transients and noted that the breakdown track appears under the microscope as a thin strip of a metallic-appearing substance between the two metallizations. From examinations of microsections of flash-across shorts he concluded that metal from the contacts arcs across the junction to cause permanent damage. He proposed that the breakdown track is caused by a dielectric breakdown along the interface between the silicon and silicon dioxide. He mentioned that fast rise-time voltage pulses could create sufficiently high fields across the junction, before the depletion region can reach its equilibrium width, to initiate a dielectric breakdown in the interface in the region where the junction intersects the silicon surface. He reported that the breakdown track could be reproduced by discharging a capacitor across a reverse-biased p-n junction and that the capacitance required to cause breakdown is a function of the separation of the

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* This failure mode may also occur in planar transistors. Because of geometrical considerations, the breakdown track is found only to occur across the emitter-base junction.

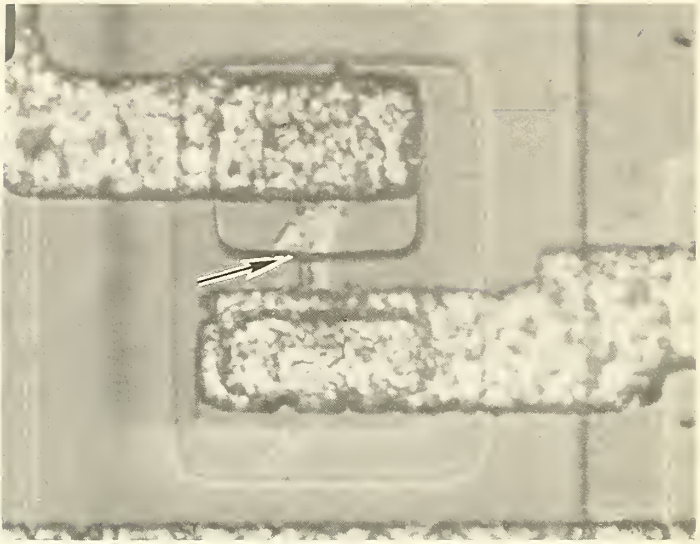

Figure 11. Photomicrograph of a breakdown track which appears as a localized surface irregularity connecting the emitter and base metallization contact stripes in an integrated circuit. (Magnification 1240 X).

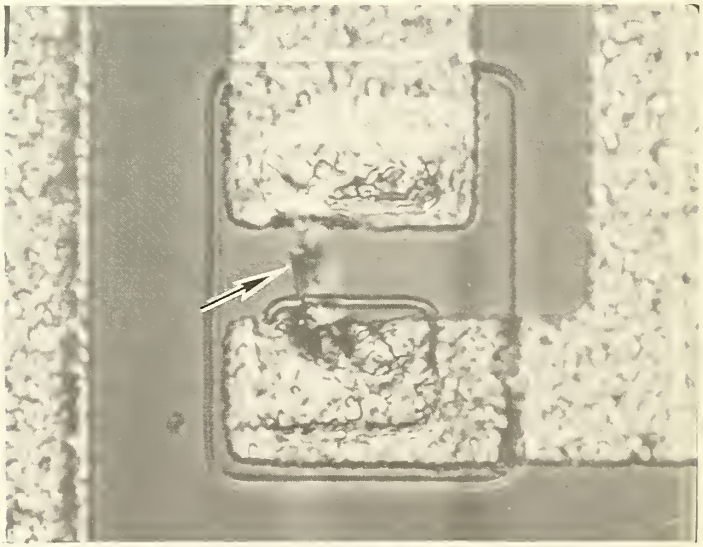

Figure 12. Photomicrograph of a breakdown track which appears as a pale-white smear connecting the emitter and base metallization contact stripes in an integrated circuit. (Magnification 1240 X).

adjacent metallization stripes and of the dielectric strength of the interface. However, he showed no data to support these reported observations.

Smith [1] has reported the results of stressing many integrated circuits with voltage pulses to selected terminals. These circuits had been fabricated with a variety of technologies: junction or dielectric isolation, glassivated or nonglassivated surfaces, and diffused or thin-film resistors. He found that 98 percent of the microcircuits subjected to high-voltage pulses 0.1 to 10 μs in duration failed via the breakdown tracks which he called junction shorts. He maintains that this failure is caused by the initiation of second breakdown in reverse-biased junctions and that the tracks lie in the bulk silicon but near the interface between the silicon and silicon dioxide. In support of this contention that the breakdown track was in the silicon and not at the interface, he showed that the width of the breakdown track broadened somewhat and then narrowed as layers of the silicon in the area of the breakdown track were removed by etching. However, it is not clear why an interface-initiated event could not also have produced damage in the silicon bulk. Apparently his reason for citing second breakdown as the failure mechanism is evidence of localized heating. Smith concluded, from an electron beam analysis (x-ray mode), that for short pulse durations of about 1 μs or less, no aluminum had migrated into the breakdown track from the aluminum contacts. Smith also concluded that the method of sintering the aluminum metallization to achieve contact to the silicon could have a significant effect on the energy level at which circuit failure caused by junction shorts would occur. He recommended a low-temperature, short-time alloying procedure to avoid nonuniform alloying into the silicon bulk which would tend to concentrate the current and lower the resistance of the circuit to failure.

Two other papers have dealt with similar failure modes. Knudsen [3] reported seeing metallic bridging shorts extending across p-n junctions beneath the silicon dioxide to connect the adjacent aluminum contacts in dielectrically isolated integrated circuits which had incurred this damage and failed during electrical testing. He was able to reproduce such failures in nondegraded devices by connecting one of the terminals to a voltage source having no current-limiting resistance to simulate a situation which could have occurred in testing if the device had mistakenly been rotated by 180 deg before being inserted in the test jig. The polarity of this voltage was such that the p-n junctions where the breakdown tracks occurred were stressed with a forward bias. These "metallic bridges" were about 10 μm in width and extended about 6 μm deep into the silicon. Knudsen proposed that the conduction track had apparently developed a molten channel of aluminum and silicon beneath the thermal oxide. Lytle and McAteer [4] reported seeing such metallic tracks, which they called white spears, across junctions stressed with reverse-bias voltage pulses of millisecond duration. For reverse-bias voltage pulses of microsecond duration,

they saw no white spears but rather a cracking of the thermal oxide and an alloying of the aluminum metallization contacts with the underlying silicon at the ends of the breakdown track.

In the present study, breakdown tracks were seen across junctions which had been stressed with reverse and with forward bias voltage pulses of 0.025 to 1.0 μs duration. In some of these cases, a pale-white smear along all or a portion of the breakdown track was seen; this observation suggests the possibility of some migration of the aluminum. Earlier work by Harman [6] on a surface breakdown phenomenon produced by sub-microsecond-duration high-voltage pulses on special-geometry silicon diodes did reveal migration of aluminum among breakdown tracks consisting of a line of craters about 10 μm in diameter as far as 200 μm from the aluminum contacts. Each crater is believed to have been the result of one pulse. While this surface breakdown may or may not be related to the present failure mode, the study lends credence to the possibility of aluminum migration in a microsecond time-frame.

Recently, Lane [5] reported some exploratory studies of breakdown tracks on special test patterns involving *p-n* junctions and diffused resistors. He called the breakdown tracks surface overstress failures or, simply, surface zaps. He proposed that the mechanism responsible for the breakdown tracks is surface related and involves field enhanced migration of the metallization-metal-and-silicon eutectic along a line determined by the electric fields and the crystallographic directions in the silicon. The <100> direction was the preferred direction for the surface breakdown tracks observed by Harman [6]. It is interesting to note that the projection of the <100> direction is along the <211> direction that Lane reported to be the preferential direction for the breakdown tracks he observed in the {111} silicon surface. Lane also reported that such factors as the silicon resistivity, junction geometry, metallization-electrode stripe spacing, oxidation and metallization-alloying temperatures all have an effect on the stress level at which breakdown tracks are initiated. Most of Lane's results, however, are for relatively long pulses, the shortest of which is 50 μs. He did suggest that his proposed mechanism would be valid for pulses as short as 1 μs but that below this level there may be a transition to another mechanism. Lane recommended that more sophisticated experiments be performed to quantify his results and to determine the limits of the silicon technology with respect to these voltage overstress failures.

A breakdown track in monolithic integrated circuits can also result from r-f stress. Roe and coworkers [7] reported that r-f pulses* of sufficient power coupled directly into the output of quad, two-input NAND gates resulted in a collector-to-emitter short circuit of the output transistor caused by what they called a lateral

* pulse duration: 500 μs; frequency: 0.22 to 9.1 GHz.

spike of aluminum and damaged oxide extending directly from the collector contact to the nearest emitter contact. They concluded from this failure mode that the output transistor had been driven into second breakdown by the r-f pulse which thereby caused localized heating and a lateral channel of molten silicon mixed with aluminum from the aluminum contact stripes.

In summary, the situation is one in which there is relatively little information available that can be used to understand what is, perhaps, the most prevalent failure mode of monolithic integrated circuits exposed to voltage transients. Only one exploratory study of the initiating conditions at the metallization stripes affected has been reported. The other studies reported have dealt only with the conditions at the terminals to the circuit for which the circuit fails. Two contrasting failure mechanisms have been proposed: one suggests a surface-related and the other a bulk-related phenomenon. As yet there is insufficient evidence to determine which and under what conditions either mechanism may or may not apply.

(H. A. Schafft and W. K. Croll)

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This quarterly progress report, seventeenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include design of a plan to provide standard silicon wafers for four-probe resistivity measurements for the industry, publication of a summary report on the photoconductive decay method for measuring carrier lifetime, publication of a comprehensive review of the field of wire bond fabrication and testing, and successful completion of organizational activity leading to the establishment of a new group on quality and hardness assurance in ASTM Committee F-1 on Electronics. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; and measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes. New efforts were initiated in both the die attachment and wire bond evaluation tasks. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes. A description of breakdown tracks, a primary failure mode of monolithic integrated circuits stressed with voltage pulses, is given in a separate appendix.

17. KEY WORDS (Alphabetical order, separated by semicolons) Aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); recombination centers; resistivity; ribbon wire bonding; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; trapping centers; ultrasonic bonding; wire bonds.

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